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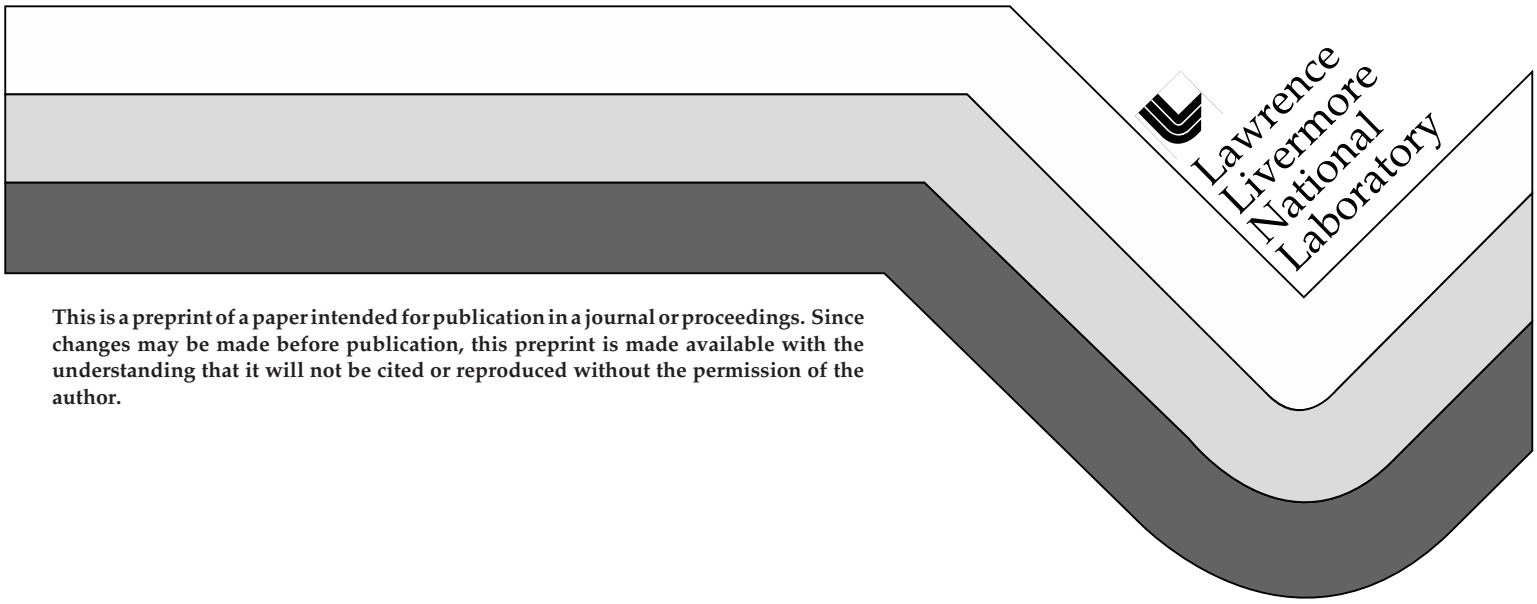

Nano-structure Multilayer Technology Fabrication of High Energy Density Capacitors for the Power Electronic Building Block

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Abstract

Commercially-available capacitors do not meet the specifications of the Power Electronic Building Block (PEBB) concept. We have applied our proprietary *nanostructure multilayer materials* technology to the fabrication of high energy density capacitors designed to remove this impediment to PEBB progress. Our nanostructure multilayer capacitors (NMCs) will also be a enabling technology in many industrial and military electronics applications. Examples include transient suppression (*snubber capacitors*), resonant circuits, and DC filtering in PEBB modules. Additionally, weapons applications require compact energy storage for detonators and pulsed-power systems. Commercial applications run the gamut from computers to lighting to communications. Steady progress over the last five years has brought us to the threshold of commercial manufacturability. We have recently demonstrated a working dielectric energy density of >11 J/cm^3 in 20 nF devices designed for 1 kV operation.

Objective

Power electronic circuit implementations are currently limited by capacitor size and performance. Only incremental improvements are anticipated in existing capacitor technologies, while significant performance advances are required in energy density and overall performance to meet the technical needs of the applications which are important for U.S. economic competitiveness. One development program, the Power Electronic Building Block (PEBB), is seeking an electronics revolution in power electronic design. High energy density capacitors with excellent electrical thermal and mechanical performance represent an enabling technology in the PEBB concept because current capacitor technology does not meet requirements on volume, operating temperature, and other important specifications.

Our program applies LLNL's *nano-structure multilayer* technologies to the development of high voltage, high energy density capacitors. Our controlled sputter deposition techniques are capable of synthesizing extraordinarily smooth micron-thick layers of dielectric and conductor materials. We have demonstrated that, with this technology, high voltage capacitors with at least an order of magnitude improvement in energy density are achievable. Well-understood dielectrics and new dielectric materials are being investigated for use with this technology.

There are many advantages to capacitors produced by nano-structure multilayer technology. They are inherently solid-state, monolithic devices, exhibiting superior mechanical and thermal properties when compared to conventional electrolytic, polymer, or ceramic construction. Their compact, flat profiles are well-suited to surface mounting and to integration into the packages of power semiconductor devices, offering performance,

volume, and cost advantages over discrete capacitors. Later in this paper, a conceptual capacitor design for a *snubber* application will be discussed to illustrate capacitor design techniques, materials, and the performance expected with this technology.

Our long-term plans, with sufficient funding and the help of industrial partners, include NMC dielectric materials research; engineering design and evaluation for power electronics applications; building a prototype manufacturing capability for NMC production; designing a full-scale manufacturing system; and moving this technology to industry for commercial production.

Technical Problem

Rugged, high-performance, high-voltage capacitors are needed in many industrial and military applications. In the PEBB application, they are needed in at least two specific areas:

• *Snubber capacitors* associated with switching devices, such as IGBTs and MCTs. High-amplitude, high-frequency transient currents—as high as 40 A/ns—must be absorbed. This demands capacitors with the lowest possible effective series resistance (ESR) and effective series inductance (ESL). Close associating with the semiconductor die implies very high operating temperatures, on the order of 200 °C for silicon, and higher for future silicon carbide devices. Additionally, the latest concepts in resonant converter topologies require low (or at least highly repeatable) capacitance temperature coefficient.

• *Filter capacitors* on the DC power bus. High capacitance and high energy density is desired to maximize noise and ripple rejection, and particularly to reduce volume. Again, low ESR and ESL are important.

These applications require high-voltage, high energy-density capacitors with good circuit performance. LLNL's NMCs have strategic advantages when compared to existing technologies. Current capacitor technologies suffer from defects and inhomogeneity included in the dielectric material and introduced during capacitor manufacturing which contribute to reduced voltage breakdown. Important voltage breakdown mechanisms include electronic or avalanche breakdown, electrochemical breakdown and thermal breakdown as dielectric loss increases under intense electric field stress, temperature, and with aging.

In the snubber application, the current choices are polymer film and ceramic capacitors. Polymer films such as polypropylene are characterized by low loss, high breakdown voltage, but low dielectric constant. Film capacitors suffer from material and manufacturing defects such as pinholes and particle contamination, and can fail under mechanical and thermal shock. High temperature (200 °C) operation is impractical. They are bulky and are not expected to achieve the performance required for PEBB systems.

Capacitors based on mixtures of ferroelectric ceramic dielectrics such as $BaTiO_3$ have a much higher dielectric constant, but a lower intrinsic breakdown voltage than polymer materials. Performance of today's ceramic capacitors, though much improved in recent years, is still limited by ceramic powder quality, capacitor design and the manufacturing process. There are thermal and mechanical problems with the larger ceramic devices, making them difficult to solder and unreliable after many temperature cycles. Dielectric loss and the associated heating is an issue with the highest energy density compositions, such as X7R. High cost is also an issue.

Nanostructure Materials Background

Nano-engineered multilayer materials are characterized by a near-atomic scale and thus, uniquely large interfacial area to volume ratios [1]. Successful capacitor structures fabricated using multilayer technology will give us the ability to engineer high performance capacitors. We can optimize properties by materials selection, design of the synthesis process, and

materials processing. Multilayer materials are widely known in the materials community for scientific study and physics application. Their use has been demonstrated at many laboratories, including LLNL. The multilayer effort at LLNL is among the strongest in the world as it is a core technology supporting many programmatic and scientific activities [2].

Nano-structure or nano-phase multilayer materials are dense, low contamination solids synthesized using atom by atom processes. They are characterized by a high concentration of material interfaces. The most notable of such materials are semiconductor superlattices fabricated using molecular beam epitaxy (MBE). However, multilayers may be synthesized using elements from all parts of the Periodic Table using MBE, evaporation, sputtering and electrochemical deposition technologies. At this time, multilayer structures have been fabricated by physical vapor deposition from at least 75 of the 92 naturally occurring elements in elemental form, as alloys or as compounds. The structure of multilayer materials is determined in synthesis by control of the thicknesses of the individual layers during deposition. These thicknesses vary from one monolayer (0.2 nm) to thousands of monolayers (>1000 nm).

Until recently, the macroscopic thickness of nano-structure multilayer materials has been generally limited to less than a few microns, and more typically to 0.5 μm or less. Recently, processes for deposition of thick macroscopic nano-structure multilayer materials have been developed at LLNL and used to fabricate free standing high quality structures up to 300 μm thick containing up to 50,000 individual layers. Our existing research synthesis system produces samples having periods uniform to 2% of the individual layer thickness and areas of ~ 100 cm^2. These macroscopic nano-structure multilayer samples enable use of standard diagnostic techniques for material property characterization and open a path to develop devices with performance that approaches theoretical limits.

The through film and lateral perfection of these macroscopic multilayer materials have been determined using surface roughness measurements, cross-section transmission electron microscopy (TEM) and standard x-ray diffraction analysis. The surfaces of macroscopic multilayers (t > 20 μm) have demonstrated surface perfection essentially equal to the substrate roughness: multilayers deposited on super polished substrates with roughness of ~ 0.02 nm RMS and 0.14 nm peak to valley (PV) had roughness of ~ 0.04 nm and 0.29 nm PV. Cross-section TEM shows that the multilayer structure ~17 μm from a substrate is identical to that 1 μm from that same surface and that this uniformity extends laterally over several microns. X-ray analysis demonstrates that the multilayer period of a 5 nm period 25 μm thick free standing structure varied by less than 1% top to bottom through 10,000 individual layers and is constant over 10 cm on single substrates. The perfection shown by these characterization results is unique in that it is atomic in scale but extends over macroscopic thicknesses. These materials exhibit exceptional application specific performance as a result of their nano-structures and atomic distributions. Structural flaws that characteristically limit performance are controlled so that the full potential of the nano-structure multilayer materials is achievable.

There are several potential advantages inherent to fabrication of high energy density capacitors by multilayer synthesis technologies. First, the processes used are generic in that a wide range of materials may be deposited as thin films. Therefore, it will be possible to apply new materials as they are developed, potentially enhancing the dielectric properties of the insulating spacer (i.e. *technology insertion*). The designs presented here are based on simple metaloxide dielectrics, particularly Ta_2O_5, with a dielectric constants of k=27 and a maximum breakdown strength of V_b = 4 to 6 MV/cm. Recent work with material mixtures (proprietary at this time) indicate that a dielectric constant in the range of 100 is feasible without performance penalties.

Breakdown strengths of complex dielectric materials in thin film form are not currently well known but are expected to be substantially larger than those observed for commercial bulk materials formed using powder compaction/sintering processing (~0.1 MV/cm). This optimistic opinion is based on our ability to fabricate fully dense layers having controlled

surface roughness less than 5 Å on a routine basis. This is demonstrated in Figure 1 where a cross section transmission electron micrograph of an Al-Al_2O_3 multilayer having a periodicity of 920 Å is shown at a magnification of 100,000x.

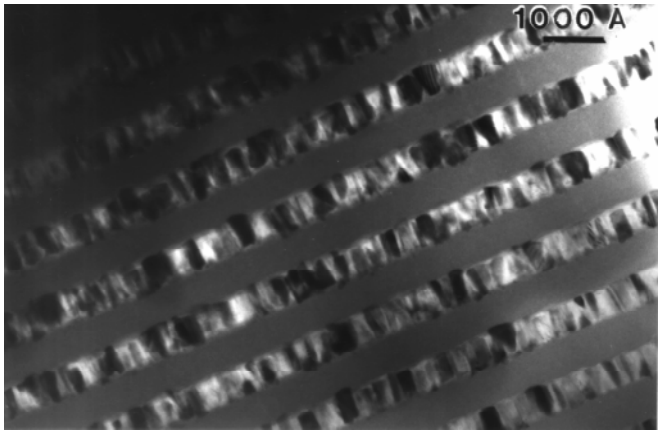

Figure 1. Transmission Electron Microscope (TEM) image of an Al/Al2O3 multilayer. In this case, the crystalline aluminum conductor layers and amorphous alumina dielectric layers are both 460Å (0.046 μm) thick. Surface roughness at the interfaces is 10 Å rms.

Note the uniformity of the layers and the interfacial quality; the interfaces in this structure are smooth to approximately two to four atomic diameters (5-10 Å). Second, these structures are thermally and mechanically robust. Strengths approaching the theoretical limits of the component materials in metal/metal multilayers have been experimentally demonstrated for several alloy systems. Also, these materials are observed to be stable in multilayer form to temperatures in excess of 500°C in most cases. Thus, nano-engineered multilayer structures have several strategic advantages in developing high performance capacitors.

Capacitor Fabrication Process

Capacitors are fabricated by magnetron sputtering from metal targets through a shadow mask onto a substrate (Fig. 2). Within the sputtering chamber, there are typically two or more sputtering sources to permit interlayering of various materials—for instance conductor and dielectric materials, the minimum for a typical capacitor. Dielectrics are formed by reactive sputtering in the presence of oxygen at a rate of 20 Å/s for Ta_2O_5; 70 Å/s has been demonstrated for Al_2O_3. By repositioning the mask in the plane of the substrate, an overlapping pattern may be formed with alternating despositions of metal and dielectric as shown in Fig. 3. This concept quickly leads to a near-net form capacitor with a large number of possible layers [3,4].

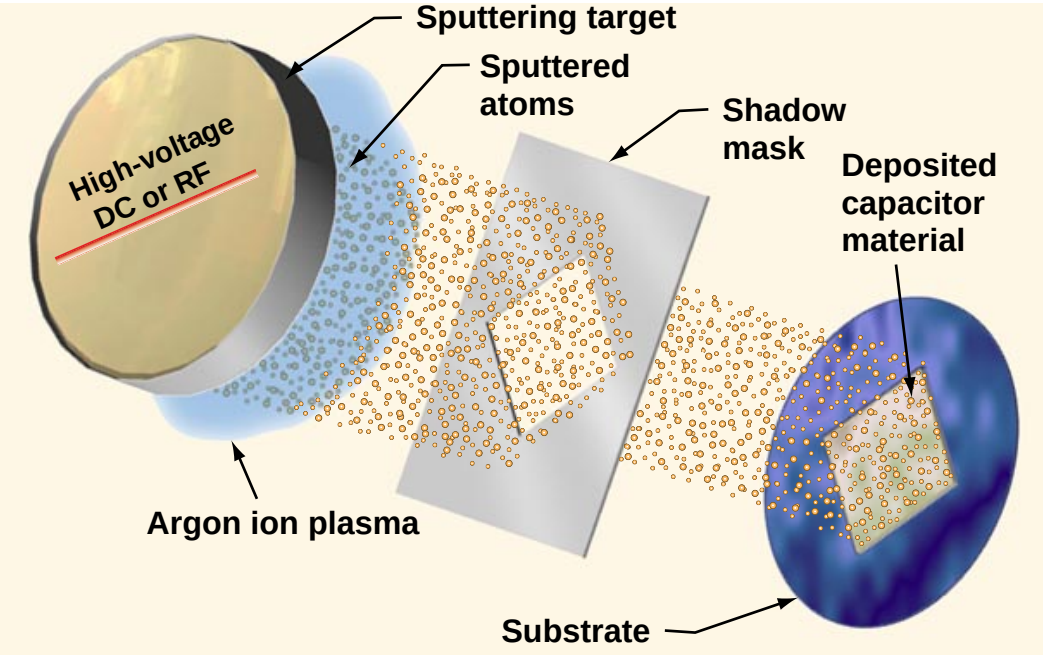

Figure 2. Sputtering with a shadow mask produces a capacitor structure.

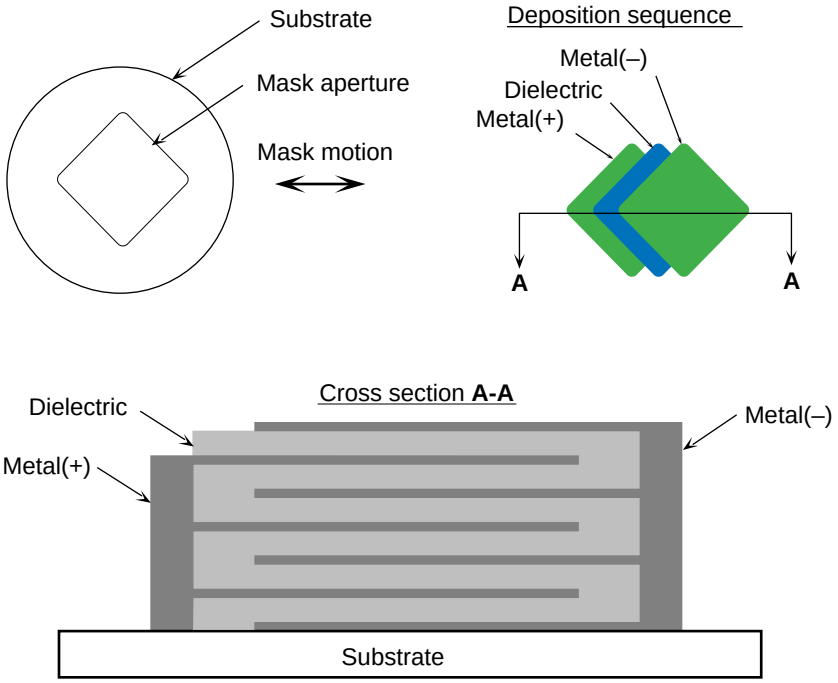

Figure 3. Shuttling the mask produces a layered capacitor structure on the substrate.

Because of the very thin dielectric layers, breakdown performance modes are expected to improve. One effect, avalanche breakdown, is reduced because of rapid electron recapture. In ordinary foil capacitors, breakdown at the edges of the foils is a nagging problem. In our NMC design, the edges, or plate tips, can be completely buried in the solid dielectric. Electromagnetic modeling [5] indicates that full burial reduces field enhancement by 15%. This has been demonstrated in practice on single-layer test capacitors with Al_2O_3 dielectrics.

The choice of substrate materials is flexible, with the major requirement being smoothness. We generally use alkali-free borosilicate glass (Shott AF45) originally developed for the flat-panel display industry. Surface roughness was Ra = 2 Å RMS over a 100 μm distance as measured on a Wyko interferometer and confirmed with high-resolution TEM. This glass is low in cost and available in thicknesses from 50 μm to 1.1 mm. Since it is an insulator, contact with the bottom electrode must be made along the edges, in the same manner as the top electrode. Sapphire is another good choice, having a low coefficient of thermal expansion, high strength, and smotth surfaces available. Substrate cleanliness is also extremely important, both for film adhesion and for freedom from defects due to particulate contamination.

Masking is one of the challenges in the fabrication process. One or more masks must be precisely located in intimate contact with the substrate for each deposition step. The mask(s) must be easy to replace and fairly low cost, even for a research system. Also, the masking apparatus must operate within the vacuum chamber, which limits the choice of materials and fabrication methods. We are using an automated apparatus that meets the needs of multilayer capacitors masking for experimental-scale production. Stepper and servo motors move the actuators under computer control. The measurement and control system enables us to program the deposition sequences and automatically record important parameters for later analysis.

The NMC manufacturing process is environmentally benign. Solid metal or ceramic materials are deposited in a vacuum chamber. Waste materials are predominantly metals in solid or oxide forms. The resulting capacitors are solid-state with no seals to fail or corrosive fluids to leak. They are expected to have excellent mechanical and thermal properties: resistance to vibration, stress, and elevated temperatures.

An NMC Snubber Capacitor Design

We introduce a conceptual design addressing a snubber capacitor designed for use with high-frequency switching semiconductors. Compatibility with surface mounting or other low-inductance interconnections is mandatory. Integration of the device into the conceptual PEBB switch module interconnect structure would offer a significant improvement in performance and a cost saving when compared with externally-mounted ceramic capacitors. The goal here is to design a 0.2 μF, 1200 V device. ESR and ESL must be exceptionally low, 2 mΩ and 2 nH respectively.

This design assumes the use of a Ta_2O_5 dielectric with the working characteristics listed in Table 1. Contacts are assumed to be copper, suitable for soldering and direct mounting between bus bars. These robust connections improve the likelihood of low contact resistance and inductance while improving reliability over temperature cycling. Recent experience with pure copper has been satisfactory with respect to film roughness, adhesion, interaction with dielectrics, and solderability. We may choose to use a multilayer conductor to optimize the ESR, thermal coefficient of expansion, tensile strength, or other material parameters.

Table 1. Working characteristics for Ta_2O_5.

Working E field intensity	3 MV/cm (8 kV/mil)
Dissipation factor (*Tan δ*)	.003
Relative permitivity (*k*)	27
Dielectric energy density	11 J/cc
Temperature coefficient of *k*	20 ppm/°C

Capacitor dimensions are driven by two major factors: energy density of the dielectric and resistance of the conductor. Energy density is very high for NMC dielectrics—more than an order of magnitude improvement over the best ceramics. For this example, the stored

energy requirement at 1200 V is 144 mJ, implying a dielectric volume of 0.013 cm^3. Dielectric thickness, driven by its breakdown strength, must be at least 4 μm. Therefore, the total dielectric area must be 33 cm^2. The finished capacitor form factor is of course flexible, but assume for this example that it is about 2 cm square. The required number of dielectric layers is then eight.

Effective series resistance for this capacitor is determined primarily by the bulk resistance of the copper, though it is also influenced at high frequencies by skin effect and dielectric loss. Measurements have been performed on 1 cm square single-layer NMCs that indicate that, for low frequencies, the bulk resistance formula ($R = \rho\, l / a$) is accurate. To achieve an ESR of 2 mΩ, the total copper thickness must be about 20 μm, or 2.2 μm per conductor layer. The total thickness of the capacitor materials is now 32 + 20 = 42 μm, plus substrate thickness. The packaged energy density is determined primarily by the substrate volume for a device of this size.

Inductance of a thin parallel-plate capacitor is extremely small because the magnetic fields in adjacent plates cancel one another. We have measured a self-resonant frequency of 30 MHz on a 23 nF, 2.5 cm square device, corresponding to an ESL of 1.3 nH. That inductance is similar to that of a sheet conductor with those dimensions. Note that small inductances are challenging to measure, being dominated by instrumentation connections; the same is true of interconnection effects in real applications.

A summary of specifications for this design appears in Table 2. Using our current estimates for large-scale production, this capacitor should cost about one dollar to produce.

Table 2. Snubber capacitor specifications.

Capacitance	0.2 μF
Working voltage	1200 V
Maximum energy storage	140 mJ
Dimensions	2 x 2 x 0.042 cm + substrate
Effective Series Resistance	2 mΩ
Effective Series Inductance	1 nH

This conceptual design uses novel materials to engineer an extraordinary capacitor. Alternative material choices for dielectrics will certainly improve these specifications. High energy density, low loss, good thermal and mechanical properties, and low inductance make the nanostructure multilayer capacitor an excellent candidate for power electronics applications.

Technical Status and Issues

We have made significant progress in the fabrication of NMCs. The high dielectric deposition rates required for economical manufacturing are projected to be greater than 30 Å/s (0.18 μm/min). This is achieved in our work using a unique reactive sputtering process developed at LLNL. The acceptable range of process parameters is also broad, indicating that process scaling is possible.

Our process yield is driven primarily by microcontamination control, just as it is in the semiconductor industry. External contamination sources include substrate cleanliness, preparation of the sputtering system, and the usual cleanroom controls. Internal contamination can arise from the sputtering cathode, process gasses, and shielding. We are addressing each of these contamination sources with good success. Industry-standard process yield models for large-area semiconductor devices [6] provide a good empirical fit to our data and indicate continuing yield improvement. We now routinely produce single-layer devices with areas of 6 cm^2 at a yield of 25% with respect to achieving the required working voltage.

Some important technology issues remain to be investigated. Time-dependent dielectric breakdown of nano-structure multilayer capacitors needs to be well understood for a variety of materials and capacitor designs. Interfacial reactions (e.g., diffusion) between dielectrics and conductors are important to understanding voltage breakdown phenomena. Complex-composition dielectrics may offer advantages. Thermal expansion characteristics—particularly related to interconnection methods— requires continuing study.

Other engineering issues include optimal substrate choice and substrate removal to fabricate free-standing capacitors. Full capacitor performance characterizations need to be done. Additional work must be done on mechanical properties and interconnection for integration into power electronics modules. Scale up of this nano-structure capacitor technology will require investment in facilities and equipment, and will present new fabrication and processing problems.

Future efforts, in cooperation with our industrial partners, will include the design and construction of a scaled-up capacitor fabrication facility, design and testing of commercially-practical capacitors, and the design of high-volume manufacturing equipment for industry. LLNL is pursuing several industrial contacts who have expressed interest in manufacturing NMCs.

The PEBB design team at Harris Semiconductor Corporation believes that a commercially-viable NMC technology will have a major impact on PEBB objectives, and on the future of power electronics in general. Expected NMC characteristics—high energy density, high performance and reliability, and competitive cost—make NMCs an enabling technology. Harris will test laboratory prototype NMCs under realistic conditions to evaluate transient discharge performance and reliability. They will also supply design requirements and evaluate design tradeoffs to integrate NMCs into the PEBB package.

Related Ongoing Work at LLNL

LLNL is an applied physics laboratory with a well-established materials and engineering technology base. We draw on the collective capabilities and expertise at LLNL to better understand power electronics applications and be in the best position to meet our industrial partners' capacitor performance goals. Some core materials technologies include the nano-structure multilayers, interatomic materials diagnostics, and carbon and silica Aerogels. Multilayers are currently being developed as physics diagnostic and optical devices. Research is proceeding to take advantage of their remarkable mechanical and thermal properties for DOE programs and applications in aerospace and related industries. Transmission electron microscopes, x-ray diffraction, and similar diagnostic capabilities at LLNL are needed tools to understand and develop nano-structure multilayer materials.

LLNL also has well-developed engineering thrust areas in pulse power, microwave, laser and semiconductor technologies, and electromagnetic and device modeling. Very large capacitor banks have been developed for electric gun, rail gun and x-ray applications. LLNL originated the concept of small pulse-power slapper detonators for weapon initiation. Microwave broad band sources and vulnerability assessment at LLNL rely on high performance capacitor technology. Pulsed, high power lasers developed at LLNL for DOE and DoD programs similarly rely on high performance capacitors banks. Research has been done on laser and electron beam initiated fast semiconductor switches for pulse power applications. Our electromagnetic and device modeling expertise is a resource used by DOE and DoD programs.

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